

**REMARKS**

Claims 1-20 were pending in this application.

Claims 1-20 have been rejected.

Claims 1-4, 6, 7, 9, 10, 12, 14, 15, and 17-19 have been amended as shown above.

Claim 21 has been added.

Claims 1-21 are now pending in this application.

Reconsideration and full allowance of Claims 1-21 are respectfully requested.

**I. REJECTION UNDER 35 U.S.C. § 102**

The Office Action rejects Claims 1-20 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,648,281 to Williams et al. ("*Williams*"). This rejection is respectfully traversed.

A prior art reference anticipates the claimed invention under 35 U.S.C. § 102 only if every element of a claimed invention is identically shown in that single reference, arranged as they are in the claims. MPEP § 2131; *In re Bond*, 910 F.2d 831, 832, 15 U.S.P.Q.2d 1566, 1567 (Fed. Cir. 1990). Anticipation is only shown where each and every limitation of the claimed invention is found in a single prior art reference. MPEP § 2131; *In re Donohue*, 766 F.2d 531, 534, 226 U.S.P.Q. 619, 621 (Fed. Cir. 1985).

Claim 1 recites that a "trench" is etched in a "substrate" between a "first area" for forming a base and an emitter of a bipolar transistor and a "second area" for forming a sinker and a collector of the bipolar transistor. Claim 1 also recites that a "portion of [the] substrate" in the "second area" is doped to form a "sinker and collector layer comprising a sinker portion and

a collector portion.”

*Williams* recites techniques for forming various types of transistors, diodes, resistors, and other elements simultaneously in an integrated circuit chip. (*Abstract*). Numerous figures in *Williams* illustrate the use of transistors. However, *Williams* never recites that a trench is formed in a “substrate” as recited in Claim 1. Instead, *Williams* simply recites that the substrate is doped to form various types of “buried layers” (denoted “B.L.”, “PBL”, or “NBL”). *Williams* never recites that the actual substrate itself is etched to form a trench as recited in Claim 1.

*Williams* also recites the use of “sinters” in various types of transistors. However, *Williams* never recites that the sinters are formed by doping a portion of a substrate. Rather, *Williams* repeatedly shows the sinters being formed in other areas of an integrated circuit, such as in an epitaxial layer. As a result, *Williams* never recites doping a “portion of [a] substrate” in a “second area” to form a “sinker and collector layer comprising a sinker portion and a collector portion” as recited in Claim 1.

For these reasons, *Williams* fails to anticipate the Applicant’s invention as recited in Claim 1 (and its dependent claims). For similar reasons, *Williams* fails to anticipate the Applicant’s invention as recited in Claims 9 and 17 (and their dependent claims). Accordingly, the Applicant respectfully requests withdrawal of the § 102 rejection and full allowance of Claims 1-20.

## II. NEW CLAIM

The Applicant has added new Claim 21. The Applicant respectfully submits that no new matter has been added. At a minimum, the Applicant respectfully submits that Claim 21 is

patentable for the reasons discussed above. The Applicant respectfully requests entry and full allowance of Claim 21.

**III. CONCLUSION**

The Applicant respectfully asserts that all pending claims in this application are in condition for allowance and respectfully requests full allowance of the claims.

**SUMMARY**


If any issues arise, or if the Examiner has any suggestions for expediting allowance of this application, the Applicant respectfully invites the Examiner to contact the undersigned at the telephone number indicated below or at *wmunck@davismunck.com*.

The Applicant has included the appropriate fee to cover the cost of one additional dependent claim. The Commissioner is hereby authorized to charge any additional fees connected with this communication (including any extension of time fees) or credit any overpayment to Deposit Account No. 50-0208.

Respectfully submitted,

DAVIS MUNCK, P.C.

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William A. Munck  
Registration No. 39,308

P.O. Drawer 800889  
Dallas, Texas 75380  
(972) 628-3600 (main number)  
(972) 628-3616 (fax)  
E-mail: *wmunck@davismunck.com*